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Proceedings of the 22nd IEEE Asian Test Symposium (ATS'13) Yilan, Taiwan, 18-21 November 2013

doi: <http://dx.doi.org/10.1109/ATS.2013.53>

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Preprint

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Accurate Multi-Cycle ATPG in Presence of X-Values

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Abstract—Unknown (X) values in a circuit impair test quality and increase test costs. Classical n -valued algorithms for fault simulation and ATPG, which typically use a three- or four-valued logic for the good and faulty circuit, are in principle pessimistic in presence of X-values and cannot accurately compute the achievable fault coverage.

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For the first time, accurate deterministic ATPG for multi-cycle test application is supported for stuck-at faults. Experiments on ISCAS'89 and industrial circuits with X-sources show that this new approach increases the fault coverage considerably.

Index Terms—Unknown values, test generation, ATPG, QBF, multi-cycle, partial scan

I. INTRODUCTION

Unknown values, also called X-values, adversely affect the quality and cost of VLSI test [1]. X-values may be caused for example at A/D boundaries, clock domain crossings, or at uninitialized memory blocks or flip-flops as found in partial scan designs.

X-values reduce signal controllability and observability. Consequently, circuit testability and fault coverage is reduced. The propagation of X-values in a circuit can be controlled by additional X-blocking design-for-test hardware which increases area and performance cost.

If response compaction is used (e.g. in embedded deterministic test or built-in self test), special handling of X-values in the compactor is necessary to avoid compromising the response signature. X-tolerant compactors [2], X-canceling time compactors [3] or structures for X-masking [4] can be used.

In partial scan circuits, where non-scan sequential elements have an unknown state, faults may require multiple test cycles to be detected [5, 6] even though a single test cycle is sufficient for detection in the full-scan circuit. In *scan-per-test* [6], all scannable elements are loaded with test stimuli. The non-scan elements are assumed to have unknown values (otherwise complex design-for-test hardware is necessary to keep stable values during scanning). Then one or multiple primary input patterns are applied in subsequent test cycles without intermediate scanning.

Test pattern generation for such multi-cycle tests for partial scan circuits was proposed in [7] based on random patterns and fault simulation. This technique is limited because it generates

unnecessarily long test sequences and fails to generate patterns for hard-to-test faults. Also, it cannot prove fault untestability.

In partial scan circuits, multiple cycles can be used to initialize non-scan elements. In contrast to an uninitialized sequential element, the general case of an X-source is more difficult to handle since it generates a new (unique) X-value per cycle. In this case, multi-cycle tests still increase fault coverage if fault activation or propagation requires reconvergences involving X-values.

Standard n -valued ATPG algorithms use a limited set of values for the good and faulty circuit [8]¹ and cannot accurately reason about such X-reconvergences. The underlying, limited n -valued symbol set does not allow to distinguish different X-values. Fault simulation and ATPG algorithms that *accurately* take X-values into account in *single-cycle* tests have been proposed in [9, 10]. These algorithms are based on Boolean and quantified Boolean satisfiability and significantly increase fault coverage compared to standard three-valued ATPG algorithms.

Here, we propose the first accurate stuck-at fault multi-cycle ATPG algorithm for partial-scan circuits and circuits with X-sources in general. The proposed ATPG is able to accurately classify all faults for a given maximum number of time frames. In particular, we provide:

- Fault activation and propagation conditions that must be considered during deterministic multi-cycle test generation in order to classify faults accurately.
- An algorithm for exact test pattern generation and computation of fault coverage for multi-cycle test which is complete compared to previous ATPG based on random patterns [7]. It is also able to find the shortest test pattern sequence and applicable to larger circuits.
- A thorough investigation of the fault coverage increase in presence of X-values when multiple cycles are used for fault activation and propagation.

The next section introduces the terminology and Section III presents fault detection cases to be considered during accurate multi-cycle test generation in presence of X-values. Section IV describes the proposed accurate multi-cycle ATPG approach. The increase in fault coverage of the multi-cycle test and accurate reasoning is shown by experimental results in Section V.

II. TERMINOLOGY AND PROBLEM STATEMENT

Signals at which unknown or X-values originate are called X-sources. X-sources at primary inputs generate a unique X-value in each cycle whereas uninitialized (non-scan) sequential elements generate a unique X-value in the first time frame. An X-value is one of the two values logic 0 or 1, but it is not known which of the two.

¹In the following, these algorithms will be referred to as three-valued algorithms.

A fault depends on X-sources if the support of the fault-site, i.e. the union of input cones of the outputs reachable from the fault-site, contains at least one X-source.

In a circuit with X-sources, we define a fault as detected if the fault effect is visible as binary difference at the *same* observable circuit output in the *same* time frame, independent of the actually generated values at the X-sources. This detection requirement is a modification of the detection requirement for partial scan circuits of [6], which also allowed that the fault effect is observable at different outputs or different time frames, depending on the state of the non-scan flip-flops. The method proposed here can be easily extended to support this as well.

A detecting test is a pattern specifying the value of the scannable elements and one or multiple patterns for the primary circuit inputs such that the fault is detected.

III. MULTI-CYCLE FAULT DETECTION IN PRESENCE OF X-VALUES

The detectability of faults influenced by X-sources depends both on the accuracy of the ATPG algorithm as well as the test application. A stuck-at fault may be untestable in a single-cycle test, but become testable if multiple time frames are considered. This section describes cases requiring both multi-cycle test and accurate reasoning in presence of Xs to activate faults or propagate their effects for detection to the outputs. These cases must be taken into account by any multi-cycle ATPG algorithm that aims at an accurate and complete modeling of fault activation and propagation in presence of unknowns under consideration of multiple time frames. While we focus on the stuck-at fault model, the reasoning is also applicable to test generation for other fault models, such as transition delay faults.

A. Multi-cycle Line Justification Using X-Blocking

In classical X-aware ATPG algorithms (e.g. based on the three-valued logic [8]), line justification in the output cones of X-sources for fault activation and error propagation requires the blocking of X-values by use of controlling values of gates along their propagation path. Depending on the fault-site, the X-sources and the circuit, the justification of required values for fault detection may be impossible in a single cycle and the fault is classified as untestable although it may be detectable when multiple cycles are considered.

Figure 1 a) shows a sequential circuit with a non-scan flip-flop, which leads to an X-value at signal c . If only a single time frame is considered, the ATPG algorithm cannot justify any logic values at signal c and signal h . In consequence, at least the stuck-at faults at these signals are classified as untestable. This is illustrated in Figure 1 b).

However, if multiple time frames can be used during test application, the search space for line justification grows and values can be justified not only in the first but also in subsequent time frames. This additional freedom may allow test generation for faults (otherwise untestable) by using several time frames in order to block X-values introduced by uninitialized flip-flops.

For the fault h -stuck-at-1 in the example, the consideration of two time frames allows to generate a valid test pattern as shown in Figure 1 c).

In multi-cycle test generation, a valid test pattern requires that the fault effects in preceding time frames are taken into account

properly even if the fault is activated in later time frames. This requires special modeling as explained in Section IV.

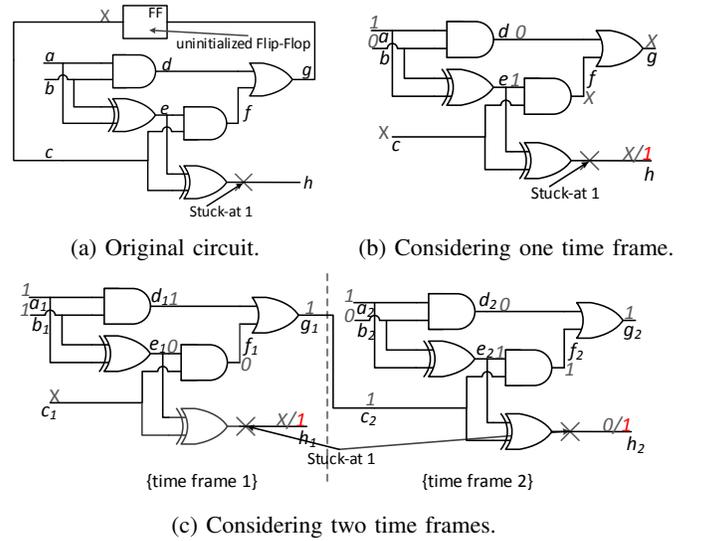


Fig. 1: Circuit with uninitialized flip-flop and fault h -stuck-at 1.

B. Fault Detection Using Controlled X-Reconvergence

Classical multi-valued ATPG algorithms are pessimistic when considering X-values and fail to accurately track X-values and their reconvergences. This is even more pronounced in multi-cycle tests when fault detection may require to distinguish between correlated and uncorrelated X-values and their reconvergence for fault activation and propagation in one or multiple time frames in the good or faulty circuit. Imagine a simple XOR-gate with two inputs having an unknown value. An ATPG algorithm based on three-valued logic will only determine that the output shows an unknown value. In contrast, if it is known that these X-values are correlated since they originate from the same source, and for example always have the same logic value, the output of the gate can be accurately evaluated to logic 0.

In the following the different X-reconvergence situations in multi-cycle testing that require accurate reasoning to generate test patterns for targeted faults are described in detail:

1) Controlled X-Reconvergence in Separate Time Frame:

Figure 2 a) shows a sequential circuit with one X-source at line a (e.g. an uninitialized flip-flop) and a stuck-at 0 fault at signal b . In this case, the X-dependency of the fault-site causes that in the faulty circuit, signals e and h evaluate to X for all possible input assignments. As a consequence, this fault is untestable if only one time frame is considered (Figure 2 b)).

However, using a second time frame and accurate reasoning, a test pattern can be generated as shown in Figure 2 c). Here, accurate reasoning allows to force output h_2 in the second time frame to take different binary values in the good and faulty circuit (0/1) so that the fault is detected. This is achieved by the reconvergence of the X-values of signals e_1 and h_1 (first time frame) at signal h_2 (second time frame).

2) Fault Activation in Multiple Cycles: Figure 3 shows a circuit with fault b -stuck-at 1. Again, the fault effect of the first cycle is only observable as an X-value and its inversion at signals e_1 and h_1 and needs to be propagated along multiple paths. In addition, fault propagation by X-reconvergence requires to

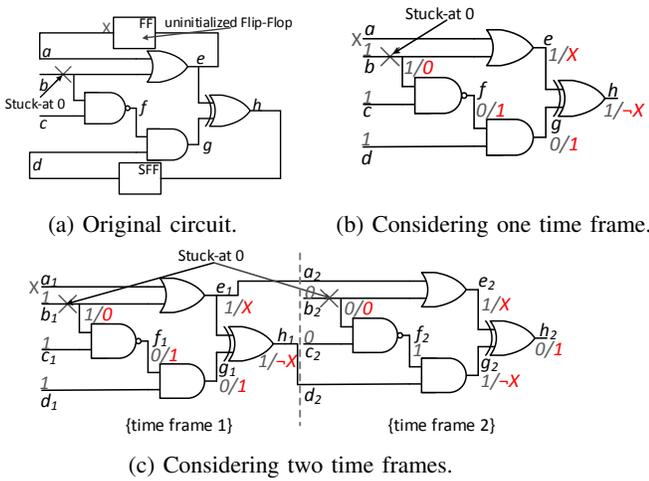


Fig. 2: Circuit with fault signal b stuck-at 0.

activate the fault also in the second cycle. Signal b_2 needs to be set to 0 to enforce the X-reconvergence and propagation to h_2 . This requires that the fault effects in the first and all subsequent frames are correctly reflected in the ATPG circuit model.

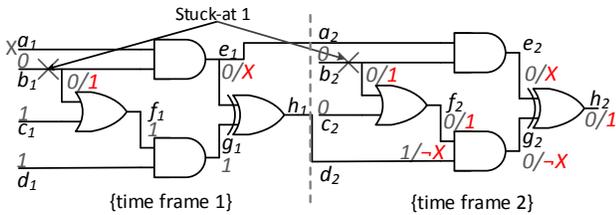


Fig. 3: Fault only detectable if justified twice.

3) *Fault Propagation Through Faulty Gate*: Special consideration in the modeling is also required if the fault effect can reach the fault-site in a later time frame. Figure 4 shows a sequential circuit with an X-source at signal a and the stuck-at 0 fault at input b of gate F . Note that different to an uninitialized flip-flop, this X-source generates a new, unique X-value in each considered time frame.

In each time frame in which the fault is activated, the fault effect is combined with an X-value. To detect the fault, these values need to reconverge. This in turn requires the propagation through the faulty gate itself, as shown in Figure 4 c). The modeling of the faulty gate must allow such behaviour.

4) *Fault Activation in Different Cycles Depending on X-Values*: Depending on the circuit, there may be a fault which cannot be activated in the same time frame for all possible assignments to the X-sources. This fault can still be detected using a single test pattern if for each X-assignment the pattern activates the fault (in different time frames) and propagates the resulting effect to the same observable output in the same observed time frame (according to Section II)². If the observation conditions are relaxed and the fault effect is measured in different time frames or at different outputs depending on the X-assignment [5], fault coverage potentially increases further.

While these cases show the need for accurate reasoning about X-reconvergences in the faulty circuit, X-reconvergences may

²Due to space limitations, we omitted a separate example for this case.

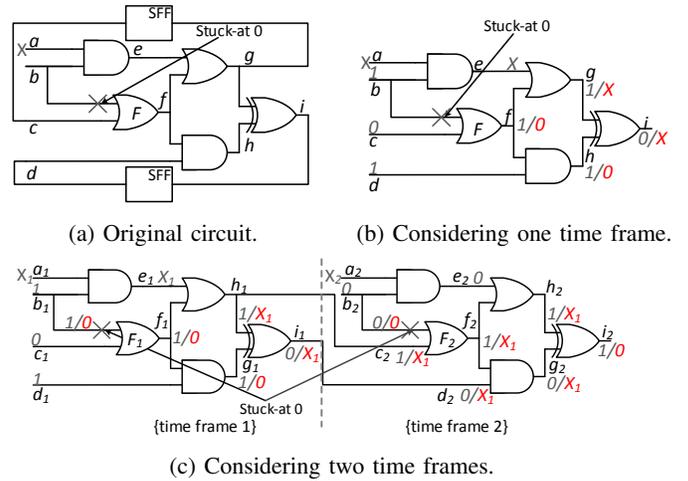


Fig. 4: Circuit with input b of gate F stuck-at 0.

also be required in the good, or both in the good and faulty circuit. Standard ATPG algorithms fail to generate tests for faults discussed above.

C. Provenly Untestable Faults in Multi-Cycle Tests

During test generation, a subset of the yet undetected faults can be marked as untestable independent of the number of considered time frames:

- 1) The testability of faults which are independent of X-sources (i.e. faults whose support does not include any X-sources) can be computed in a single time frame [6] since the test conditions are identical to these of classical full-scan ATPG. Faults which do not depend on X-values in a time frame and which are activated in that time frame but no test pattern in that frame exists, are untestable since no additional information can be gained by considering additional time frames.
- 2) Faults whose fault-site does not depend on Xs in one time frame and which cannot be activated in that frame are untestable.
- 3) Faults directly depending on a primary (non flip-flop) X-source are untestable since fault activation cannot be enforced.

The classification of these faults as definitely undetectable is mandatory in order to classify all faults in a circuit accurately.

IV. ACCURATE MULTI-CYCLE ATPG ALGORITHM

This section describes a novel deterministic multi-cycle ATPG algorithm able to accurately reason about fault detectability in presence of X-values. It takes into account the constellations discussed in Section III which are not considered in state-of-the-art structural or SAT-based ATPG systems.

The proposed ATPG algorithm extends the algorithms presented in [9, 10] to allow accurate multi-cycle test generation and fault simulation, as well as to increase runtime efficiency. The fault simulation algorithm in [9] computes the exact fault coverage of a test set in presence of X-values free of any simulation pessimism. The work in [10] is the first accurate ATPG system in presence of X-values. It combines SAT- and QBF-based reasoning to classify all faults in the combinational core of a circuit as detectable or to prove them untestable.

In this work, the two- and three-valued SAT-based ATPG of [10] is replaced by a combined two- and three-valued multi-cycle SAT approach. The QBF-based test generation is used to accurately, i.e. non-pessimistically, reflect multi-cycle fault activation and propagation. The SAT-based fault simulation of [9] is extended in order to allow the simulation of multiple time frames and to keep the runtime as low as possible.

The test generation starts with the multi-valued SAT-based ATPG to generate multi-cycle test patterns for all faults detectable using X-blocking (Sec. III-A). This corresponds to the capabilities of commercial and academic ATPG tools based on n -valued logics. Faults that are not detected and not proven undetectable according to Section III-C are processed with the QBF-based ATPG. Accurate multi-cycle fault simulation is used to implement fault dropping.

A. Combined Multi-valued Multi-cycle SAT-based ATPG

In the combined SAT-based ATPG, a two-valued encoding is used for all signals which do not depend on X-sources, and a three-valued encoding (using two binary variables per signal) for all other signals. This way, the significantly larger size of a pure three-valued instance encoding is avoided. A similar hybrid modeling is used in [11]. This leads to a CNF representation which (empirically) is up to 60% smaller and typically easier to be analyzed by a SAT solver than a pure three-valued representation. Runtime is reduced by up to 20%.

Test patterns for stuck-at faults for a given maximum number of time frames are generated in an iterative approach: Initially a SAT instance considering only the good and faulty circuit in the first time frame is constructed. If the fault cannot be activated at the fault site or is not observable at any of the outputs, a new instance is constructed which tries to activate and propagate the fault in a later time frame. This requires to consider the fault effect and all resulting dependencies of earlier time frames correctly.

Figure 5 shows fault f which should be activated and propagated to an output in the second time frame. In classical SAT-based modeling, it is sufficient to construct models of the good circuit and the output/propagation cone of the fault. However, multi-cycle test generation requires modeling of an additional output cone to represent the state of all signals affected by the fault in earlier time frames. The propagation cone for the fault effect in the currently considered time frame is used to incrementally propagate the fault effect to the outputs of the considered time frame along D-chains [12].

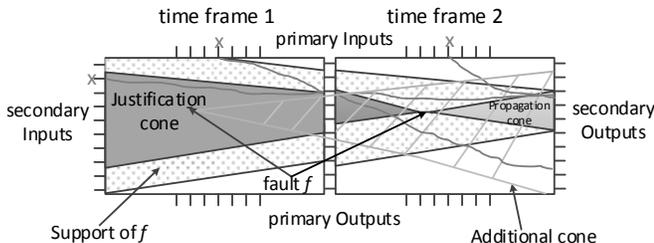


Fig. 5: Fault f activated in the second time frame.

This iterative approach is sufficient to correctly classify all faults *detectable by a three-valued ATPG algorithm*. The limited accuracy of three-valued modeling causes that if a fault effect is

not deterministically observable at the outputs of the time frame the fault is activated in, it will also not be observable in any following time frames. This is because X-reconvergences are evaluated pessimistically in the three-valued model. However, it is indeed possible that a fault effect influences fault activation or propagation in a later time frame as shown in Section III.

If the combined SAT-based ATPG fails to find a test pattern within the given maximum number of time frames, the fault is aborted and later analyzed by the QBF-based multi-cycle ATPG.

B. QBF-based Multi-cycle ATPG

The QBF-based approach is used to generate a test pattern or prove the untestability of all yet unclassified faults. For each not yet classified fault, a problem instance representing all time frames, fault effects and activation and detection conditions according to the discussion in Section III is created as quantified Boolean formula (QBF) and evaluated by a QBF solver. This allows to generate test patterns for faults for which SAT-based or single-cycle QBF-based test generation fails.

The original circuit representation is expanded to multiple time frames using an iterative logic array (ILA) representation. To generate the QBF instance, a CNF formula is generated which correctly describes all considered time frames of the expanded circuit in the good and in the faulty case.

In contrast to the instance in [10], we extended the activation and fault detection conditions to represent the test requirements for multiple time frames presented in Section III as follows: First, fault activation is allowed in any considered time frame, but the fault is required to be activated at least once for each X-assignment. Furthermore, for all time frames the fault effects in earlier time frames need to be considered properly. Since it is possible that an activated fault of one time frame propagates through a faulty gate in a later time frame, the faulty gates themselves are modeled such that fault effects of earlier time frames are taken into account. Finally, the constraint that the fault effect is always visible at the same output is extended such that for all possible assignments to the X-sources, the fault is always visible in the same time frame.

All variables used within the CNF formula need to be properly quantified. In particular, we search for *one* test pattern that satisfies the CNF formula for *all* possible assignments to the X-sources. If the solver finds such a satisfying assignment, the fault is marked as detected. Otherwise, the fault is marked as untestable in the considered number of time frames. This classification is valid since our QBF approach is able to accurately represent the behaviour of X-values. Additionally we are symbolically describing all required multi-cycle fault activation and propagation conditions.

V. EVALUATION

The proposed method has been applied to sequential IS-CAS'89 and industrial circuits provided by NXP. All measurements were conducted on a single core of an Intel Xeon CPU running at 3.3 Ghz. We use the incremental SAT solver Antom [13] and an extended QBF version of Antom, named Quantum. In the circuits, the flip-flops are modeled using pseudo-primary inputs. We assume that a fixed and randomly selected subset of

the primary and pseudo-primary inputs are X-sources³. Selected *primary* inputs generate a unique X-value in each cycle, selected *pseudo-primary* inputs are considered uninitializable non-scan flip-flops. The other inputs are controllable or become scan-flip-flops.

For each circuit and subset of X-sources, different numbers of time frames are evaluated using the collapsed set of stuck-at faults. The results show the rounded average over five ATPG runs per circuit with different sets of X-sources.

Experimental Results

Figure 6 compares the fault coverage of accurate and SAT-based (three-valued) multi-cycle test generation for circuit *s05378* considering up to nine time frames and 5% of the inputs selected as X-sources. For an ATPG based purely on three-valued logic, the consideration of a second time frame already increases fault coverage by 11.88%. However, using an accurate approach and more time frames, the fault coverage increases even further. The maximum is reached at seven time frames. Here, the accurate multi-cycle approach detects **13.79%** more faults than a standard three-valued ATPG approach using a single time frame.

The accurate multi-cycle ATPG always detects more faults than the pure three-valued SAT-based approach in the same number of time frames. This increases fault coverage by 1.33% compared to the three-valued multi-cycle ATPG. The figure also shows that the number of additionally detected faults saturates quickly after three time frames. With higher numbers of time frames the runtime increases for the untestability proofs of yet undetected faults since the QBF instance grows in complexity. In our experiments, the highest increase in additionally detected faults occurred when using two time frames.

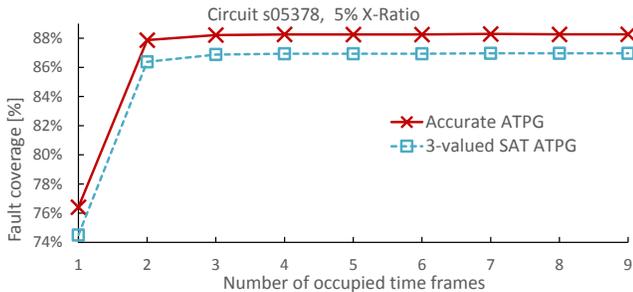


Fig. 6: Fault coverage of SAT-based compared to accurate QBF-based ATPG for different numbers of time frames

Table I shows the results of the three-valued SAT-based as well as the accurate QBF-based multi-cycle approach for the larger ISCAS’89 and NXP circuits. Based on the results shown in Figure 6, the maximum number of considered time frames was limited to three. For each circuit, the table lists the number of primary (PI) and pseudo-primary (PPI) inputs, the size in number of complex gates and the number of collapsed stuck-at faults. Per circuit, we conduct the experiments for the case of 1 and 5% of the inputs selected as X-sources (‘X-ratio’) as well as a up to three time frames (‘TF’).

³If X-sources are clustered, e.g. a data bus generating X-values, the pessimism in standard ATPG increases since the probability of detecting faults by simple X-blocking decreases. Thus, an accurate analysis would yield even better results.

For each of these cases, columns 8 to 11 contain the results of the SAT-based ATPG. Column ‘Detected’ contains all faults, detectable by a SAT-based multi-cycle ATPG within the given maximum number of time frames. Column ‘ ΔFC ’ lists the increase in fault coverage (in %) compared to a three-valued SAT-based ATPG considering only one time. Column ‘UT’ lists all faults which are marked as definitely untestable (cf. Section III-C) and column ‘Abort’ the number of faults which the three-valued ATPG was not able to classify. Note that three-valued ATPG algorithms are limited in the accuracy when X-values are present.

Columns 12 to 14 show the results of the accurate approach. Column ‘Detected’ shows all faults classified as detectable and column ‘ ΔFC ’ the increase in fault coverage (in %) compared to a SAT-based ATPG considering only one time frame. Column ‘UT’ contains all faults which were marked as untestable using the given number of time frames. These faults may be detectable using additional time frames. Finally, column ‘Abort’ contains the number of faults which the accurate approach was not able to classify within a cumulative timeout of 11 seconds. For each fault, at first a timeout of 1 second is used for classification. If a fault is aborted and not detected by fault simulation of other generated patterns, it is tried again with a timeout of 10 seconds.

The results show that the three-valued SAT-based multi-cycle approach already increases fault coverage considerably: Fault coverage increases by up to 9.65% considering two time frames and 11.32% considering three time frames. However, the accurate approach considering all constellations of Section III correctly increases fault coverage even further. For 5% of the inputs selected as X-sources, fault coverage increases by up to **4.53%** for the ISCAS’89 circuits, and by up to **3.41%** for the NXP circuits when compared to the SAT-based multi-cycle ATPG considering three time frames. In total, up to 13.47% more faults (circuit *p78k*) could be marked as detectable in comparison to a SAT-based ATPG and one time frame. This boosts fault coverage from 85.19% to **98.66%** without the need for any X-blocking or X-masking hardware. This means that the untested faults are reduced by more than 90%.

On average for 5% of the inputs selected as X-sources and a maximum of three time frames, the three-valued multi-cycle approach classifies 9.86% more faults, and the accurate multi-cycle ATPG **12.35%** more faults as detectable compared to a standard three-valued ATPG considering only one time frame.

The last column of the table lists the runtime of the accurate approach in seconds. The runtimes increase with the number of considered time frames but are still reasonably low given the complexity of the problem.

VI. CONCLUSIONS

This paper presented a novel test generation method to increase stuck-at fault coverage in circuits with X-values due to partial scan or other X-sources. We discussed situations and techniques for multi-cycle fault detection in presence of unknown values and integrated them into an accurate multi-cycle ATPG framework in order to generate multi-cycle test patterns for stuck-at faults. Our approach is the first which is complete for the given number of considered time frames and generates test patterns for faults which neither a SAT-based nor a QBF-based ATPG detects considering only a single time frame.

Extensive experiments on standard benchmarks and larger industrial circuits demonstrate the significant increase in fault coverage not only in contrast to approaches considering one time frame, but also to three-valued SAT-based multi-cycle ATPG.

ACKNOWLEDGMENTS

The authors thank Tobias Schubert and Sven Reimer from the University of Freiburg for support with the SAT and QBF solvers Antom and Quantom. This work was partially supported by the German Research Foundation (DFG) under grants WU 245/11-1 (OASIS), BE 1176/14-2 and GRK1103.

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TABLE I: RESULTS OF 3-VALUED SAT-BASED AND ACCURATE MULTI-CYCLE ATPG FOR MAX. 3 CONSIDERED TIME FRAMES

Circuit	Inputs		Gates	Faults	X-ratio	TF	SAT-based multi-cycle ATPG				Accurate multi-cycle ATPG					
	PI	PPI					Detected	$\Delta FC[\%]$	UT	Abort	Detected	$\Delta FC[\%]$	UT	Abort	Time [s]	
s09234	36	211	5 597	13 892	1.0	1	12 390	0.00	228	1 274	12 436	0.33	1 143	0	4	
						2	12 785	2.84	228	879	12 895	3.64	767	2	72	
						3	12 786	2.85	228	879	12 899	3.67	689	76	1 109	
						5.0	1	9 841	0.00	68	3 984	10 089	1.79	3 198	0	44
						2	10 496	4.72	68	3 328	11 120	9.21	2 457	248	3 751	
						3	10 755	6.58	68	3 069	11 311	10.58	1 901	613	8 589	
s13207	62	631	7 951	20 184	1.0	1	18 980	0.00	134	1 070	18 995	0.07	932	0	5	
						2	19 141	0.80	134	908	19 184	1.01	859	7	309	
						3	19 158	0.88	134	892	19 223	1.21	646	181	3 399	
						5.0	1	15 863	0.00	125	4 196	16 392	2.62	2 869	0	10
						2	17 341	7.32	125	2 718	17 804	9.61	2 245	11	531	
						3	17 551	8.36	125	2 508	18 466	12.89	1 285	309	5 349	
s35932	35	1 728	16 065	51 649	1.0	1	45 565	0.00	3 979	2 105	45 565	0.00	1 887	0	12	
						2	46 485	1.78	3 979	1 185	46 772	2.34	898	0	48	
						3	46 647	2.10	3 979	1 022	46 861	2.51	808	0	109	
						5.0	1	41 333	0.00	1 996	8 321	41 333	0.00	7 252	0	21
						2	45 247	7.60	1 996	4 396	46 291	9.60	3 363	0	105	
						3	45 928	8.90	1 999	3 722	46 745	10.48	2 905	0	205	
s38417	28	1 636	22 179	56 605	1.0	1	54 636	0.00	295	1 853	54 658	0.04	1 640	12	175	
						2	55 136	0.88	115	1 354	55 204	1.00	1 235	51	693	
						3	55 193	0.98	115	1 296	55 531	1.58	325	633	8 379	
						5.0	1	48 083	0.00	34	8 488	48 349	0.47	6 547	84	1 257
						2	52 916	8.54	34	3 655	53 280	9.18	2 795	496	6 578	
						3	53 621	9.78	34	2 950	54 865	11.98	883	828	13 580	
p45k	1 408	2 331	39 786	107 814	1.0	1	105 570	0.00	186	2 059	105 811	0.22	1 378	20	540	
						2	107 179	1.49	186	450	107 299	1.60	174	155	2 257	
						3	107 239	1.55	186	390	107 319	1.62	73	237	3 387	
						5.0	1	91 568	0.00	92	16 153	92 830	1.17	12 392	181	3 534
						2	101 976	9.65	92	5 746	103 247	10.83	1 920	2 555	32 152	
						3	103 769	11.32	92	3 952	104 610	12.10	449	2 663	35 581	
p78k	171	2 977	74 243	225 476	1.0	1	218 945	0.00	2	6 530	222 504	1.58	1 850	129	2 108	
						2	222 705	1.67	2	2 769	224 809	2.60	424	241	3 415	
						3	223 504	2.02	2	1 971	225 092	2.73	112	270	3 459	
						5.0	1	192 074	0.00	10	33 392	208 926	7.47	10 897	806	15 989
						2	210 116	8.00	10	15 349	220 681	12.69	2 824	1 961	28 198	
						3	214 751	10.06	10	10 715	222 450	13.47	892	2 124	29 868	